Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

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**Top Material: Aluminum**

**Backside Material: Ti/Ni/Ag**

**Bond Pad Size: .045 x .045”**

**Backside Potential: Drain**

**Mask Ref: 0266**

**APPROVED BY: DK DIE SIZE .623 x .564” DATE: 7/21/21**

**MFG: IXYS THICKNESS .020” P/N: IXFD170N65X2-C9**

**DG 10.1.2**

#### Rev B, 7/1